Digital Signal Processing Solutions

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                    │    SIGNAL    │
                    │  PROCESSING  │
                    │    DOMAIN    │
                    └──────┬───────┘
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     ┌──────┴──────┐                ┌──────┴──────┐
     │  HARDWARE   │                │  SOFTWARE   │
     │  PARADIGM   │                │  PARADIGM   │
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│   ASIC    │ │ PLD/FPGA│      │   DSP   │ │   GPP   │
│(Custom &  │ │         │      │         │ │         │
│  COTS)    │ │         │      │         │ │         │
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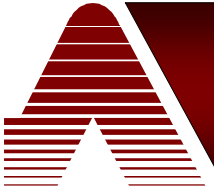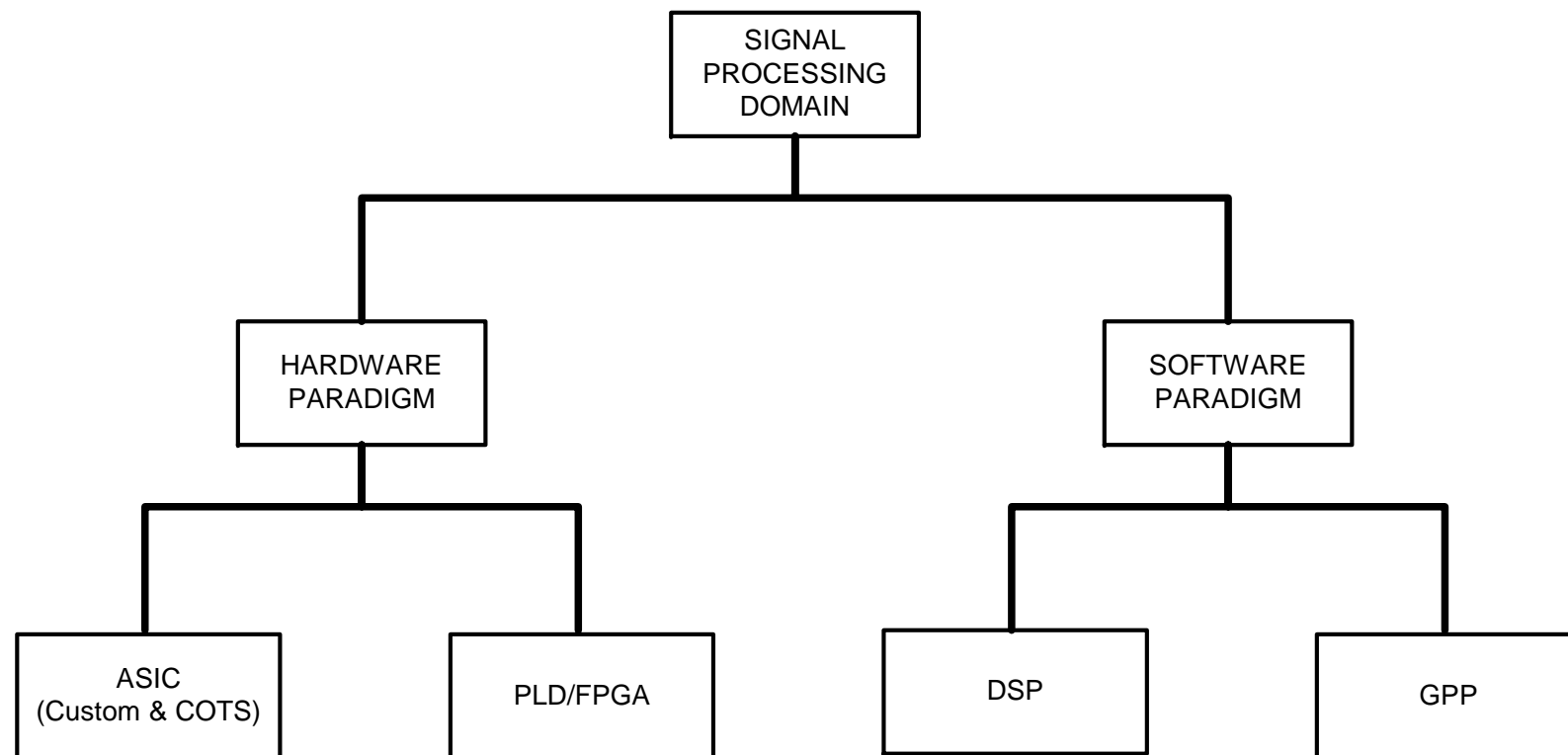
Hardware Paradigm

- **Application-Specific Integrated Circuit (ASIC)**
  - A kind of semi custom integrated circuit, often referred to as "gate-array" or "standard-cell" products, developed and designed to satisfy a specific application requirement as opposed to a general purpose circuit, such as a microprocessor.

- **Field Programmable Gate Array (FPGA)**
  - Pioneered by Xilinx as a class of programmable logic devices (PLD) that feature a gate-array-like architecture with a matrix of logic cells surrounded by a periphery of I/O cells where the interconnect mask is defined after the IC has been manufactured.

ASIC - Introduction

- **ASICs are customized or tailored to perform specific functions to a particular system or application**

- **ASICs are typically employed as bus interfaces, glue logic, functional accelerators, and/or a System-On-Chip (SoC).**

- **ASIC Types are:**
  - **Full-Custom**
  - **Standard-Cell–Based**
  - **Gate-Array–Based**
  - **Channeled Gate Array**
  - **Channel less Gate Array**
  - **Structured Gate Array**
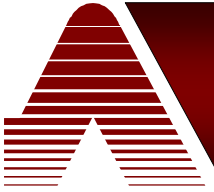
ASIC - Benefits

- Improve performance

- Reduce power consumption

- Reduce production costs

- Mix Analog and Digital Designs

- Design optimization through IC manufacturing process

- Development Tools support HDL and Schematic design approach

ASIC - Drawbacks

- **Inflexible design**

- **Higher Risk Of Obsolescence (driven by market)**

- **Large NRE (up to 16 million) from development and testing**

- **Deployed systems can not be upgraded**

- **Mistakes in product development are costly**

- **Updates requires a redesign**

- **Impediment to rapid time-to-market designs**

- **Complex and expensive development tools**

FPGA - Introduction

- **FPGA is a sub class of ASICs**

- **Matrix of configurable logic blocks (CLBs) that can implement combinational or sequential logic**

- **Provides a method for programming the CLBs and interconnects**

programmable basic logic cell

programmable interconnect
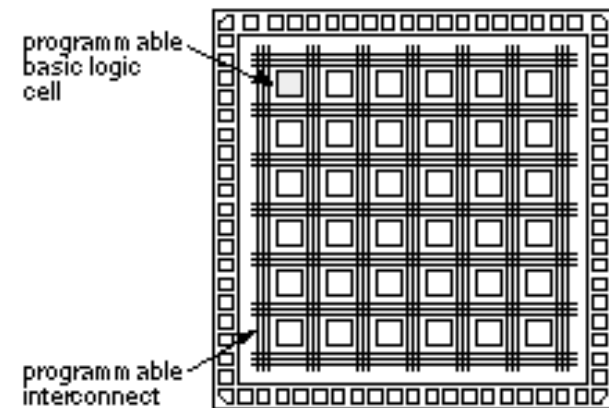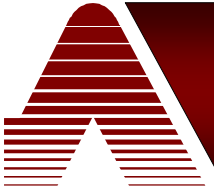
FPGA - Benefits

- **Reconfigurable / Reprogrammable Hardware**
- **Shorter development allows for fast time to market**
- **Design and debug changes can be made instantaneously**
- **Allows for:**
  - design reuse
  - parallel design
  - SOC design
- **Development Tools support HDL and Schematic design approach**
- **Offer greater performance compare to software solutions with lower clock speeds**
- **Designs started in FPGA's can be migrated to ASICs**
- **Reduces processor obsolesces**
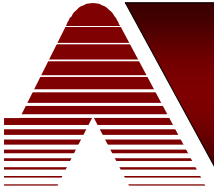
FPGA - Drawbacks

- More expensive than a ASIC on a per unit basis

- Typically have much higher power dissipation

- Un-programmed at power up

- Need a PROM or Host to store image

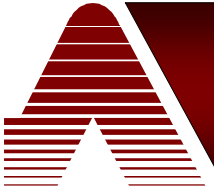- More difficult to debug compared to a software approach

Software Paradigm

- **Digital Signal Processor (DSP)**
  - A microprocessor whose architecture is specially designed for numerical computations on discrete number sequences specifically tailored to the processing of signals.

- **General Purpose Processor (GPP)**
  - A family of microprocessors and microcontrollers whose architecture are represented by complex instruction set computer (CISC), reduced instruction set computer (RISC), or the very long instruction word (VLIW). GPPs are best suited for performing a broad array of tasks that are not specifically tailored for any particular application.
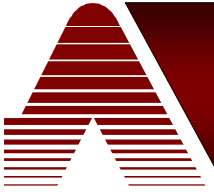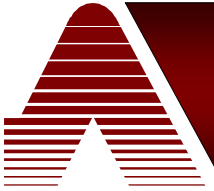
DSP - Benefits

- **Increased Performance through:**
  - Circular Buffering
  - Single-cycle MACs
  - Execution predictability
  - Dedicated fixed or floating point processors
- **Hard Real-time performance**
- **Flexible through software programmability**
- **Development and testing cycle mirrors GPP development**
- **Use standard software programming languages**
- **Low power consumption**
- **Reduced system cost**

DSP - Drawbacks

- **Increased Product Development Time and Cost**
  - Breadth and quality of development and debug tools
  - Processor ease of use
  - Availability of software libraries
  - May require use of assembly language

- **No general DSP system architecture like the personal computer (PC)**

- **Fixed point processors must deal with numeric effects**

- **Code reuse limited due lack of standard instruction set, interface, and operating system (OS)**

GPP - Benefits

- **Flexible through software programmability**
- **Reduced Product Development Time and Cost through:**
  - Large set of development and debug tools
  - Large set of commercial off the shelf (COTS) OS
  - Large set of available libraries
- **High-performance GPPs are becoming more DSP like with optimized instructions**
- **High Performance GPPs include a fixed and floating point processor**
- **Standard system architecture defined for many High Performance GPPs**
- **Large variety and wide availability of GPPs**
- **Large deployment of GPPs**

GPP - Drawbacks

- **High-performance GPPs timing behavior appears to be stochastic and can only support soft real-time performance due to heavy use of:**
  - Caches
  - Branch prediction
  - Superscalar execution
  - Data dependent instruction execution
- **Difficult to program DSP algorithms (FIRs, IIRs, FFTs)**
- **Compliers do not or partial support DSP optimization instructions**
- **Processor optimizations are highly dependent on the compiler**
- **DSP-oriented tools are rare**
- **Few DSP libraries available**
- **Higher power consumption**
- **Higher cost**
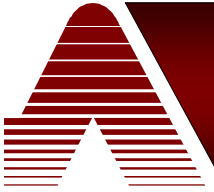
Conclusion

- **ASICs too expensive to implement on a small scale**
- **COTS ASICs subject to market demands**
- **FPGAs & DSPs have huge potential for use in deployment custom solutions**
- **GPP is effective for low rates:**
  - Use of COTS software and hardware packages
  - Large pool of knowledgeable developers
  - Rapidly deployed